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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/899,058	07/06/2001	Satoshi Inoue	110041	3173

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EXAMINER	
DOAN, THERESA T	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/899,058	INOUE ET AL.	
	Examiner	Art Unit	
	Theresa T Doan	2814	

-- The MAILING DATE of this communication appears on the cover sh t with th corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *1-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *102203* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of method claims 21-29 on 07/24/03 is acknowledged. The traversal is on the ground(s) that a search and examination of the entire application could be made without serious burden on the Examiner. This is not found persuasive, because claims 21-29 drawn to a method of manufacturing a semiconductor device, classified in class 438, subclass 149 and claims 1-20 drawn to a semiconductor device, classified in class 257, subclass 347 are drawn to distinct inventions as noted in the previous office action. Applicant's objection to the restriction requirement is noted but the fact that the two groups fall in two different classes would require two different searches and is therefore an undue burden.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21 and 28-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Makita et al. (U.S. 5,936,291).

Regarding claim 21, Makita et al. teach in figures 1A and 1B, a method of manufacturing a semiconductor device comprising a first step of forming a semiconductor layer (9,14,15) which has a source region 14, a channel region 9 and a drain region 15 on a substrate 1; and a second step of forming an insulating body 10, which has granular charge E trapping bodies inside to trap the charge of injected carriers, on the semiconductor layer (see figure 1B, column 6, lines 25-28 and lines 48-56).

Regarding claim 28, Makita et al. teach wherein the granular charge trapping bodies are silicon particles (see figure 1B, column 6, lines 25-28).

Regarding claim 29, Makita et al. teach the first step is a step to form the semiconductor layer in a low-temperature polysilicon process, thus constructing the substrate and the semiconductor layer as low-temperature polysilicon TFT (thin-film transistor) (column 11, lines 17-21 and column 6, lines 6-20).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanamoto et al. (U.S. 6,208,000) in view of Zhang et al. (U.S. 6,635,521).

Regarding claim 21, Tanamoto et al. teach in figure 6, a method of manufacturing a semiconductor device comprising a first step of forming a semiconductor layer which has a source region 6, a channel region 8 and a drain region 7 in a substrate 1; and a second step of forming an insulating body 4, which has granular charge trapping bodies inside to trap the charge of injected carriers, on the semiconductor layer (column 5, lines 42-51 and column 6, lines 31-34).

Tanamoto et al. do not teach a step of forming a semiconductor layer that has a source region, a channel region and a drain region **on** a substrate.

However, Zhang teaches the forming of a thin film transistor (TFT) having a semiconductor layer that has a source region, a channel region and a drain region on a substrate 1 (see figure 1). Accordingly, it would have been obvious to modify the transistor device of Tanamoto by forming the semiconductor layer on the substrate because as taught by Zhang, such modification would provide a thin film transistor structure, which is well known to one skill in the art.

Regarding claim 29, constructing the semiconductor layer as a low-temperature polysilicon TFT would have been obvious because as taught by Zhang, such semiconductor layer construction would provide a thin film transistor having a high performance and a low power consumption (column 1, lines 15-26).

Regarding claim 22, Tanamoto et al. further teach in figure 6 the second step comprises the steps of: forming a first insulating film 2, constituting a portion of the insulating film, on the semiconductor layer 1; depositing the granular charge 3 trapping bodies on the first insulating film 2; and forming a second insulating film 4, constituting a second portion of the insulating film, on the first insulating film 2 while the charge trapping bodies are kept on the first insulating film 2 (column 5, lines 42-51 and column 6, lines 31-34).

Regarding claim 26, Tanamoto et al. further teach the second insulating film 4 is formed by the CVD method (column 5, lines 60-62).

Regarding claims 23-24 and 27, Tanamoto et al. do not disclose the first insulating film is formed by plasma oxidation and the charge trapping bodies are formed by sputtering and etching. However, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to apply those methods in Tanamoto's structure because it is well known and commonly methods used in the art for the semiconductor thin film transistor.

Regarding claim 25, Tanamoto et al. teach that a magnetic Co particles 3 can be made of other magnetic material such as Fe, FeNi, Ni, CoPt, ect., (column 6, lines 2-4). Therefore, it would have been obvious to one having ordinary skill in the art at the time

of the invention was made to use Al-Si for the charge trapping bodies in Tanamoto's structure because Al is another magnetic material which has magnetic characteristic.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T Doan whose telephone number is (703) 305-2366. The examiner can normally be reached on Monday to Thursday from 8:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (703) 308-4918. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PHAT X. CAO
PRIMARY EXAMINER

TD
October 22, 2003.